

WHAT IS CLAIMED IS:

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1. A semiconductor memory device comprising:  
a memory cell array formed by arranging memory cells in a matrix;  
a plurality of word-lines for selecting each row of the memory cell array;  
a plurality of bit-lines for carrying data signal that is output by a memory cell belonging to each column of the memory cell array;  
a reference signal generator part for generating reference signal that is to be a reference signal when amplifying data signal occurring on the bit-line; and  
an amplifier part for amplifying the data signal occurring on the bit-line with comparing it with the reference signal,  
characterized in that the semiconductor memory device has a reference potential setup circuit part for set up potential assigned from outside of the device as potential of the reference signal.
2. The semiconductor memory device according to claim 1, characterized in that the reference potential setup circuit part comprises;  
a transistor in which a drain terminal is connected to a bit-line in the memory cell array that is a line having the reference signal, and the potential assigned from outside of the device is provided to a source terminal, and control signal activated in measurement of bit-line potential is provided to a gate terminal.
3. A testing system for testing a semiconductor memory device

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comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell  
5 belonging to each column of the memory cell array, a reference signal generator part for generating reference signal that is to be a reference signal when amplifying data signal occurring on the bit-line, an amplifier part for amplifying the data signal occurring on the bit-line with comparing it with the reference signal, and a reference potential setup circuit part for set up a  
10 potential assigned from outside of the device as potential of the reference signal, characterized in that the testing system comprises:

a reference signal control part for generating potential between source potential and ground potential with varying the potential in one direction, to apply it to the reference potential setup circuit, and controlling the  
15 potential of the reference signal;

a control part for controlling a series of steps of generating address to provide it to the semiconductor memory device and reading data signal from the memory cell;

a determination part for determining logic value of a data signal  
20 amplified by the amplifier part;

a storage part for storing potential value of the reference signal when the logic value determined by the determination part is inverted; and

a statistical process part for statistically processing the value of the potential stored in the storage part.

4. The semiconductor memory device according to claim 1 or 2, characterized in that the device comprises all or some of functions

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implemented by the control part, a determination part, a storage part and a statistical process part as set forth in claim 3.

5. A testing method for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell  
5 belonging to each column of the memory cell array, a reference signal generator part for generating reference signal that is to be a reference signal when amplifying data signal occurring on the bit-line, an amplifier part for amplifying the data signal occurring on the bit-line with comparing it with the reference signal, and a reference potential setup circuit part for set up a  
10 potential assigned from outside of the device as potential of the reference signal, characterized in that the method comprises the steps of:

(a) setting up potential of the reference signal by the reference potential setup circuit part;

(b) reading out data signal from the memory cell to the bit-line;

15 and

(c) comparing for magnitude relationship in potential, the reference signal and data signal compared by the amplifying part to obtain potential of the reference signal when the magnitude relationship inverts.

6. A semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell belonging to each column

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5 of the memory cell array, and an amplifier part for amplifying the data signal occurring on the bit-line, characterized in that the device comprises:

a signal hold circuit for taking and holding data signal read out to the bit-line.

7. The semiconductor memory device according to claim 6, characterized in that the signal hold circuit comprises a sample hold circuit.

8. A testing system for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell  
5 belonging to each column of the memory cell array, an amplifier part for amplifying the data signal occurring on the bit-line, and a signal hold circuit for taking and holding signal on the bit-line, characterized in that the system comprises:

a first control part for controlling a series of steps of generating  
10 address to provide it to the semiconductor memory device and reading out data signal from the memory cell;

a second control part for controlling such that the signal hold circuit takes data signal read out to the bit-line;

a conversion part for A/D converting data signal taken to the  
15 signal hold circuit;

a storage part for storing data signal A/D converted by the data conversion part; and

a statistical process part for statistically processing data stored

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in the storage part.

9. The semiconductor memory device according to claim 6 or 7, characterized in that the device comprises all or some of functions implemented by the first and second control parts, conversion part, storage part, and statistical process part set forth in claim 8.

10. A testing system for testing a semiconductor memory device comprising a memory cell array formed by arranging memory cells in a matrix, a plurality of word-lines for selecting each row of the memory cell array, a plurality of bit-lines for carrying data signal that is output by a memory cell belonging to each column of the memory cell array, an amplifier part for amplifying the data signal occurring on the bit-line, and a signal hold circuit for taking and holding signal on the bit-line, characterized in that the system comprises the steps of:

- (a) reading out data signal from the memory cell to the bit-line;
- (b) taking data signal read out to the bit-line, to the signal hold circuit; and
- (c) reading out potential of data signal taken to the signal hold circuit, to outside.